A Multichip Module Based RISC Processor with Programmable Hardware

Michael Newell, Wai-Chi Fang, Richard Johannesson, Icon Alkalaj
Jet Propulsion Laboratory
4800 Oak Grove Drive
Pasadena Ca. 91109

& California Institute of Technology

Abstract

A Multichip Module (MCM) based RISC processor with programmable hardware has been developed for the new era of miniaturized spacecraft required for NASA's new "cheaper, faster, better" missions.

The MCM based processor incorporates a complete 32-bit RISC computer including RAM, EEPROM and programmable hardware.

This paper describes the system architecture and its associated MCM design and implementation. It also explores the architectural merits of including user programmable hardware.

1. Introduction

A MCM based RISC processor with programmable hardware has been developed for NASA's new era of miniaturized spacecraft. The MCM based processor (MBP) incorporates a complete 32-bit RISC computer including RAM, EEPROM and programmable hardware in 1.5 cubic inches.

To further increase hardware density, die stacking technology was incorporated [l], which allows for the system memory goals to be achieved within the given volume constraints.

Not only does the presented MBP address mass and volume issues, it also uses an innovative approach to programmable hardware that allows flexibility during the processor design and implementation cycles. The programmable hardware also allows time multiplexed hardware functions [2,3] to be programmed for use in actual operation, enabling further mass and volume reductions.

In designing the programmable hardware, we introduce the concept of programmable hardware "users." We allow the programmable hardware to be accessed by both a system-user and application-users, and we look at the capabilities performed by each.

The effects on a generic computer architecture by the system-user and application-user concepts are reviewed in section 2. Section 3 discusses how the user concept impacts the MBP functional implementation. The physical implementation is also discussed. Conclusions and future work are presented in section 4.

2. Architecture

Figure 1 shows the block diagram of a generic 32-bit RISC MBP architecture with memory and programmable hardware.

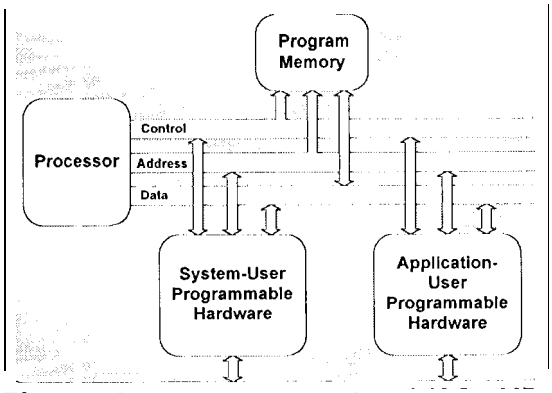

Figure 1: A Generic 32-bit RISC MB Architecture using Programmable Hardware.

2.1 Processor and Memory

MBP system capabilities depend upon 32-bit RISC processors that facilitate high data volume applications and efficient instruction execution. A flexible system should include memory partitioning that allows sufficient memory for programs, as well as access to the configuration memory of the system-user and application-user programmable hardware. Additionally, this system architecture can support any 32-bit RISC processor

by an innovative use of the system-user programmable hardware.

2.2 System-User Programmable Hardware

There are a number of distinct system hardware functions that support a modern RISC processor, including, but not limited to:

1) interfacing the processor data transfer protocol with system and peripheral hardware,

2) Memory and I/O management functions,

3) interfacing of an external data transfer protocol with the processor data transfer protocol,

4) System interrupt resource management, and

5) Specialized, system specific, hardware resources,

A number of capabilities become possible by having these system hardware functions implemented in programmable hardware. One of the significant capabilities is the ability to implement only the necessary system hardware for a specific operating environment.

External device transfer protocols can be converted to the processor data transfer protocol in the system-user programmable hardware, enabling interfaces to existing bus architectures.

Depending on the definition of system devices, control of peripherals such as mass storage, displays, etc. can be included in the system programmable hardware.

By defining a data transfer protocol for the programmable hardware composed of generic read, write, and address signals, a flexible control bus can be developed to interface to any 32-bit RISC processor. The conversion from the system processor to a generic programmable hardware control bus is consigned to the system-user.

2.3 Application-User Programmable Hardware

The application-user programmable hardware allows application users to design efficient algorithms or applications in hardware to achieve complex hardware-software co-designs.

The application-user programmable hardware also provides the flexibility for application users to implement time multiplexed hardware configuration.

3. MBP Implementation

The MBP targets space missions with requirements for 32-bit processing power and very small mass and volume. There is a strong motivation for internal programmable hardware that would eliminate external hardware implementing user I/O or specialized hardware algorithms.

The MBP incorporates TRW Inc.'s RH32 processor chipset [4,5], coupled with dic stacked RAM arrays, RAM-based FPGAs, and EEPROM for programs and FPGA configuration. This allows the MBP to obtain 20 MIPS processing power with 2.5 Mbytes of RAM, programmable system and application hardware, and 640 Kbytes of EEPROM all in a 2 by 4 by 0.25 inch package.

3.1 Functional Design

Figure 2 shows the MBP architecture implementation. The design includes usc of the RH32 chipset which provides a 32-bit RISC processor and two memory management units that implement a Harvard cache. The programmable hardware is implemented in a set of four RAM-based FPGAs [6]. The configuration for the programmable FPGAs is stored in a processor accessible 128 Kbytcs of HEPROM. The EEPROM is large enough to store multiple hardware configurations, and can be modified by the RH32 or other bus masters.

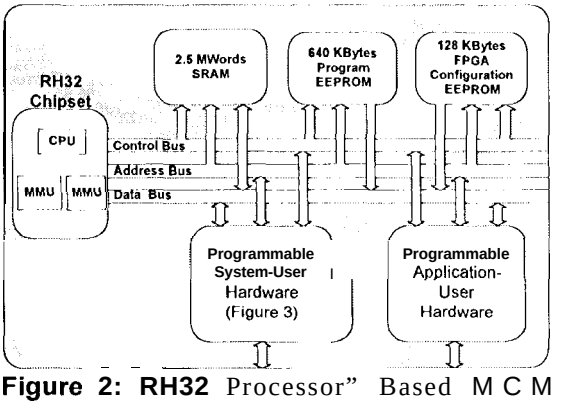

Figure 2: RH32 Processor" Based M C M Architecture

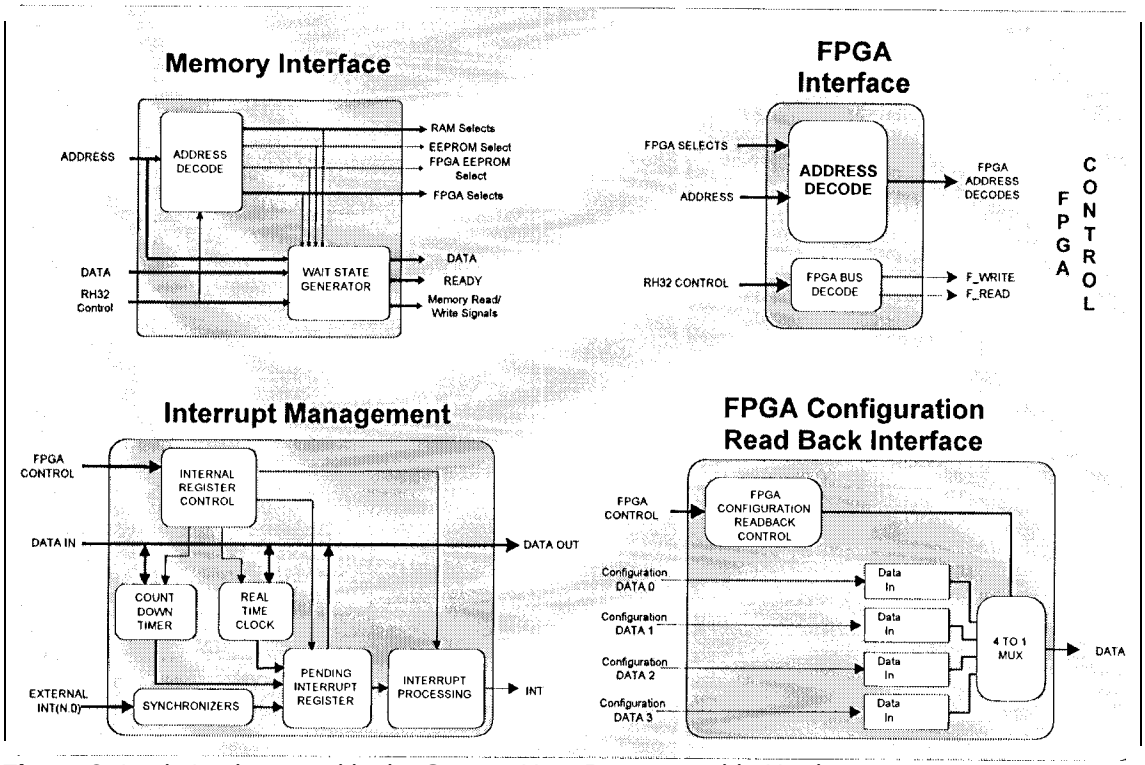

Figure 3: Logic Implemented in the System-User Programmable Hardware

The MBP has partitioned the pool of FPGAs into system and application programmable hardware. Currently 60% of the FPGAs implement system-user programmable hardware. Figure 3 shows a block diagram of the programmed system-user functions. The system-user functions include: the processor to memory interfaces, the conversion from the systcm processor control bus to the programmable hardware (FPGA) control bus, interrupt and timer management, and the FPGA configuration read back circuitry.

The first three of the above system functions are driven from modern processor support needs, the fourth is a system constraint driven by reliability concerns with a radioactive space environment. The configuration read back circuitry allows the programmed hardware to be compared with the EEPROM used to program it. This capability allows detection of changes in the RAM-based programmable hardware configuration due to Single Event Upsets (SEUs).

3.2 Physical Design

The MBP is constructed using nCHIP Inc.'s Silicon Circuit Board (SiCB). The Silicon Circuit Board is a silicon wafer with internal decoupling capacitor and routing wires deposited on silicon dioxide layers. This allows high-density interconnects between systcm components. The SiCB's integral capacitor eliminates the need for decoupling capacitor die that would otherwise use valuable die placement area. The fine interconnect wire pitch, no decoupling capacitor die, and dic stacked RAM enable the packing of 33 separate dies in the MBP. Table 1 shows the MBP physical characteristics obtained by using these approaches.

The potential problem of heat transfer in such a densely populated circuit is mitigated by use of an Aluminum Nitride package, which has excellent thermal transfer characteristics, as well as a low coefficient of expansion, that prolongs the component and interconnection life.

Mass	**100 grams**
Volume	**1.5 cubic inches (4" x 2"x 0.25")**
Number of Die	**33**
Power	6 **Watts**
Number of Package Pins	**438**

Table 1: MBP Physical Characteristics

Figure 4 shows a drawing of the completed MBP design. Figure 5 shows an actual size layout of nCHIP Inc.'s SiCB routing for the MBP with component partitions overlaid.

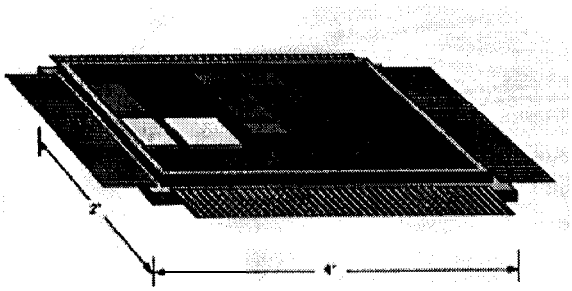

Figure 4: Final MBP Design.

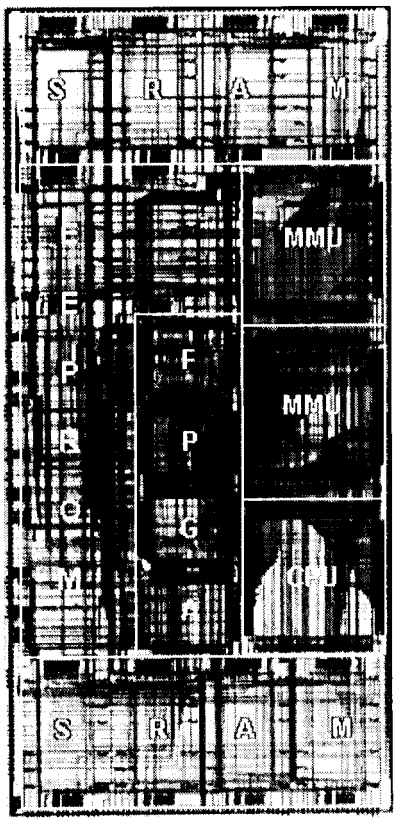

Figure 5: Actual size SiCB layout and routing with component partitioning shown.

4. Conclusions and Future Work

This first version of the MBP illustrates an order of magnitude increase in packaging density to be used by spacecraft computer hardware. Use of programmable hardware allows for greater mass and volume reduction due to not implementing infrequently used functions in permanent hardware.

By applying the "user" approach to partitioning programmable hardware, we obtain a flexible architecture for software and hardware co-design in embedded systems.

The upgrade path to a space qualifiable MBP and insertion into space applications is currently in process. This work will be incorporated in future avionics system architectures.

5. Acknowledgments

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We would also like to thank the assistance given to us by TRW Inc. on their RH32 chipset and nCHIP Inc. for their routing technology and expertise.

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